Power Factor Measurement and Correction using Digital Controller Implemented on FPGA

ArindamBiswas*, SujitDhar*,Ashoke Kumar Basu*,AmarnathSanyal*

Department of Electrical and Electronics Engineering,
Neotia Institute of Technology, Management & Science,
Jhinga; P.O: Amira, Diamond Harbor Road, South 24-Parganas,
West Bengal -743368

Abstract

Power factor is a measure of how effectively the VA – rating of electrical equipment is being utilized. A high power factor means more effective utilization. It is also beneficial from the point of view of voltage regulation and reduction in ohmic losses. Therefore PFC-devices are being widely used in industry. The simplest way to improve power factor is to insert switchable static capacitors at the receiving end of a distribution system. The paper presents a novel digital power factor correction technique using Field Programmable Gate Array (FPGA) for a system. A hardware-efficient algorithm for power factor improvement has been developed. State diagram is used to design the phase angle measurement circuit. It attempts to keep the power fact or within narrow bounds (0.95-0.97 lagging).Experimental results have been presented to show the effectiveness of the proposed technique.The general purpose SPARTANE 3AN FPGA kit has been employed for developing the digital controller. All the coding has been done using the hardware description language VERILOG.

Index Terms:

Field Programmable Gate Array (FPGA), ASIC, Feeder, Power factor correction, Static capacitor

1. INTRODUCTION

The composite load at the end of a feeder/ sub-transmission line is lagging by nature. It is due to the presence of induction motors, induction furnaces, tube-lights etc. The p.f. varies from 0.78 to 0.82 (lagging) on an average. This gives rise to unacceptably high voltage drop in the line and poor voltage regulation. Also it increases line current for the same active power and increases the ohmic losses. The counter-measure is to use power factor correction (PFC) devices. In the earlier regime, it was realized by shunt capacitors, preferably switchable, or synchronous condensers with variable excitation. Now-a-days, digital platforms are available for implementing power factor correction- these are being widely used in the industry. Our aim is to keep the effective p.f. within narrow bounds (e.g. 0.95-0.97) in spite of changes in load and its p.f. The strategy is to generate an error signal while the boundaries are crossed such that the voltage drop is within limit

and the output voltage is acceptably good in spite of continuous variation in load. With this strategy the phase difference between the input voltage and current is continuously monitored and is kept within bounds so as to achieve power factor close to unity. The switching frequency in the conventional digital power factor correction is limited because of the sampling time delay and the necessary processing time. Digital controllers provide many distinctive advantages over traditional analog control, like standard control hardware design for multiple platforms, better noise immunity, as of implementation of sophisticated control algorithms and flexible design modifications to meet a specific customer need.

The present work employs a predictive algorithm for digital power factor correction - it is derived and implemented in FPGA- platform. It provides flexibility to modify the designed circuit without altering the hardware. Concurrent operation, less hardware, easy and fast circuit modification, comparatively low-cost for a complex circuitry and rapid prototyping make it most favorable for prototyping an ASIC. All duty cycles required to achieve the near unity power factor in a half line period are generated in advance. A low cost FPGA has been used to implement PFC operating at high switching frequency.

2. FIELD PROGRAMMABLE GATE ARRAY- GENERAL DESCRIPTION

A field-programmable gate array (FPGA) is an integrated circuit which can be configured by a customer or a designer. The FPGA architecture is specified by its hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC). FPGAs of recent make have large resources of logic gates and RAM blocks to implement complex digital computations. As FPGA designs employ very fast I/O devices and bidirectional data buses, it becomes a challenging task to verify correct timing of valid data within the setup and the hold time. Floor planning enables resource allocation within FPGA to meet these time constraints. Implementation of any logical function can be made by more flexible FPGA, replacing ASIC. The ability of FPGA to update the functionality at work-site and to partially reconfigure a portion of the design as and when required is its specific advantage. Combined with its low non-recurring costs, design using FPGA is more lucrative than the earlier ASIC design (though the unit cost of FPGA is on the higher side). As such FPGAs are finding applications in power and energy systems, particularly in the field of protection. FPGAs contain programmable logic blocks. The blocks can be wired together to form different configurations. They may be configured to perform complex combinatorial functions, or merely to act as AND gate or XOR gate. In most FPGAs, the logic blocks also include memory elements, either simple flip-flops or complete blocks of memory. Some FPGAs have analog features in addition to digital. The most common features are programmable slew rate and drive strength on each output pin. Another commonly used feature is differential comparators on input pins. A few FPGAs have also analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) with analog signal conditioning blocks.

3. REACTIVE POWER CONTROL

In a radial H.V distribution or sub-transmission line, the active and reactive power drawn is dictated at the load end. As the power is fed through the line, both active and reactive power losses occur due to series impedance of the line. For short lines the capacitive effect is negligibly small. In general, the reactive losses dominate over the active losses- as such the reactive power

drawn at the load-end decides the receiving end voltage. Keeping a good voltage profile at the receiving end is always the aim of the power system engineer. Neglecting the effect of resistance which is small, the active and reactive power drawn at the load end are given as:

$$P_r \approx \frac{EV}{X_l}\sin\delta \quad \ldots\ldots\ldots\ldots [1]$$

$$Q_r \approx \frac{V_s V_r \cos\delta - V_r^2}{X_1} \quad \ldots\ldots\ldots.[2]$$

where δ is the power angle, X_l the line reactance, V_s and V_r are respectively the receiving end and the sending end voltages. The voltage drop in the line is given as: $V.D. = R\cos\phi + X_l \sin\phi$, where, R is the line resistance and ϕ, the p.f. angle. Normally, the inductive reactance of the line is much more than its resistance. As such the voltage regulation becomes poorer with lower and lower p.f. We have to increase the power factor using switchable capacitor bank so as to keep the voltage regulation within limits. The capacitor bank reduces the VAR flow by partly compensating the reactive power drawn by the load. A switchable shunt capacitor is used to improve the power factor. The phaser diagram is shown in Fig1.

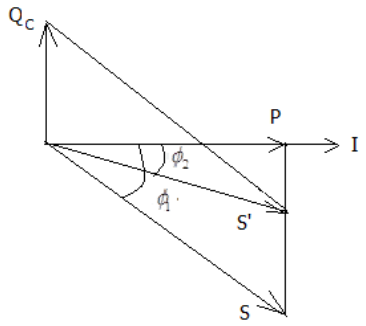

Fig1. The phaser diagram for PFC

Mathematically, the expression given for the reactive power (Q) needed to increase the electrical power factor from $\cos\phi_1$ to $\cos\phi_2$ is given as, $Q_C = P(\tan\phi_1 - \tan\phi_2)$ where P is real power demand of the load. The values of capacitance required can be calculated by using,

$$C = \frac{Q_C}{2\pi f V^2} \quad \ldots\ldots\ldots\ldots\ldots\ldots [3]$$

4. PFC UNIT

The power factor correction (PFC) device is designed to keep the p.f. angle at a relatively low value. It provides many benefits like reduction in ohmic losses by reducing the line current, reducing the line drop and improving voltage regulation etc. There are two approaches to design digital PFC unit, one approach is using block diagram method and another one is using state diagram. Fig 2 shows the circuit diagram of PFC using block diagram method wherein the

voltage signal and current signal is passed through A/D converter and then they are multiplied. The product is sent to an integrator whose output is fed to the divider circuit. The other input to the divider circuit is the product of voltage and current signal. The output of divider circuit (power factor) is sent to a Look Up Table (LUT). The output of LUT is compared with the upper and lower reference angle to decide upon whether a capacitor section has to be connected or disconnected to keep the power factor within desired bounds.This is achieved by field programmable gate array (FPGA).The general purpose SPARTAN3AN FPGA kit has been employed for developing the proto-type, with all coding done using the hardware description language VERILOG [4],[5].

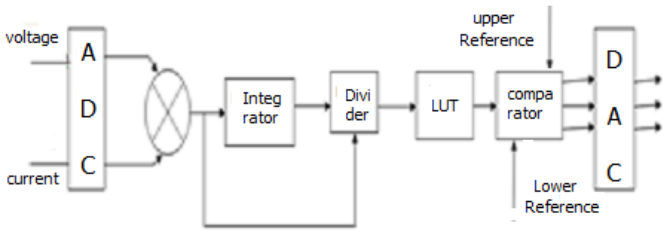

Fig.2.Simplified digital power factor correction circuit

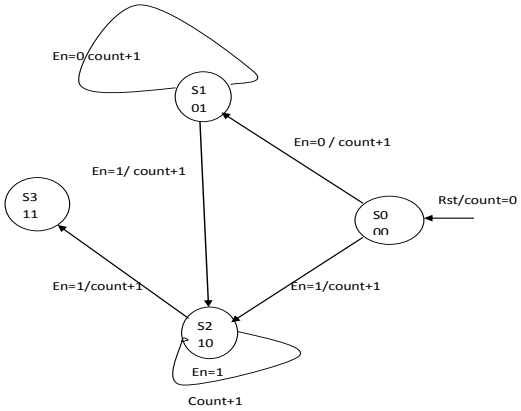

Fig.3.State diagram of digital phase angle measurement circuit

Now we developed state diagram of digital phase angle measurement circuit which is shown in Fig 3.Actually a counter is designed which counts no of sampled values of half cycle of the signal .There are four states S0,S1,S2,S3.The initial state is S0.When reset occurs then it is in the S0 state and counter become 0. Now according the value of input (EN) it will go either S1 state or

S2 state but every time counter will incremented by one .If input (En) is zero it will go S1 state and counter will incremented by one. If input (En) is one it will go S1 state and counter will incremented by one. In the S1 state, If input (En) is zero it will stay in the same state but counter will incremented by one and if input is one it will go S2 state and counter will incremented by one. In the S2 state, If input (En) is one it will stay in the same state but counter will incremented by one otherwise it will go S3 state (exit state) and counter will incremented by one.The schematic view of the digital phase angle measurement circuit is shown in the Fig 4.

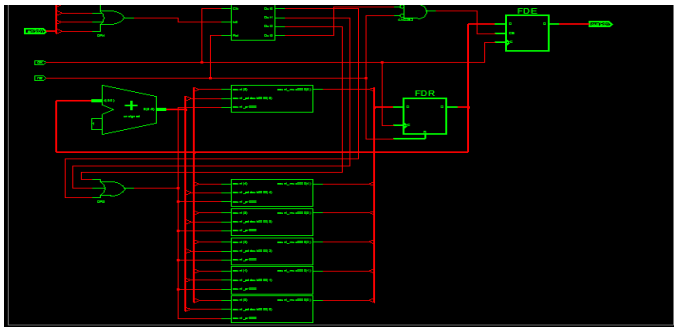

Fig.4: Schematic view of phase angle measurement circuit

5. CASE- STUDY

The case study is being conducted on a captive power plant of Western India. At full load it draws 30 Mw at 0.8 lagging p.f. from Gujarat State electricity Board. The p.f. is poor- it is aimed at enhancing the p.f. between 0.95-0.97 by using switchable capacitor operated by FPGA. The computation has been made by a specially constructed programme and the results are given below
The problem of power factor correction at the load end (captive power plant).
The power drawn by the load = (24 +j 18) MVAr
The load power factor= 0.8 lagging
The power factor angle = 36.87 ^{o}
The required power factor = 0.96 lagging
The required power factor angle = 16.26 ^{o}
The required reactive power = 7 MVAR
The reactive power compensation reqd.= 11 MVAR
Line voltage = 11 Kvat frequency = 50 Hz
Amount of capacitance reqd. = 2.89372E-04 μF
We choose capacitors of rating 33 μF, each.
The no of switchable capacitors in parallel=9

The technique:

Current signals obtained from the CTs are converted to voltages within the range compatible for FPGA kit. Now the sampled signals of voltage and current are passed through the phase angle measurement circuit and we will get different phase angle and then phase angles are fed to a

comparator which will compare both the phase angles and subtract the lower value of phase angle from the highest value of phase angle and we will get phase difference between voltage and current signal. As the FPGA kit SPARTAN 3AN contains 8 switches for inputs, 4-bit operation is done.Switches are being used as follows: Input to the FPGA chip for the present applications are clock and reset discrete voltage and current signals. The main outputs are phase difference of voltage and current signal .The schematic diagram is shown in the Fig 5. The FPGA device utilization details for the present system are shown in HDL synthesis report.

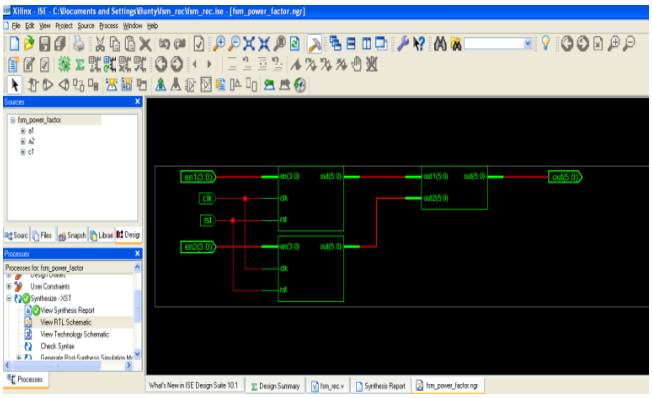

Fig.5: Schematic view of the system

6. ANALYSIS

The simulation waveforms for the digital controller for phase difference measurement circuits which are shown in Fig. 6 and Fig.7.

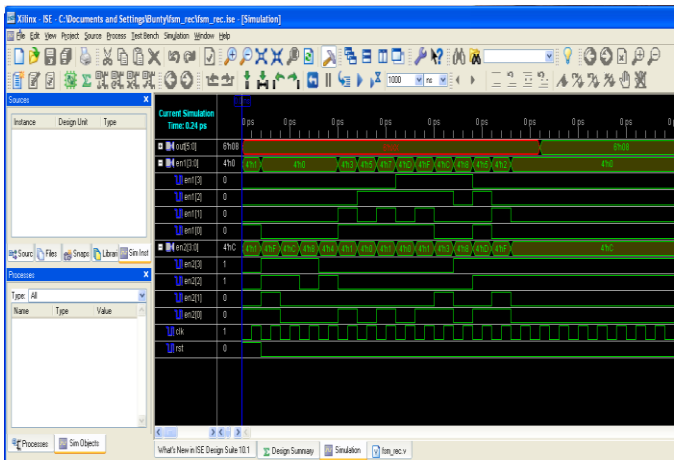

Fig.6: Simulation result of the system in ISE 10.1

From the Fig.6 , we have given to input sampled data as en1 and en2 and first counter is counted 13 sampled values and second counter is counted 5 sampled values and the difference of two counted values are 8 which is the output. The same result is shown in the simulation result in I-verilog which is in the Fig.7

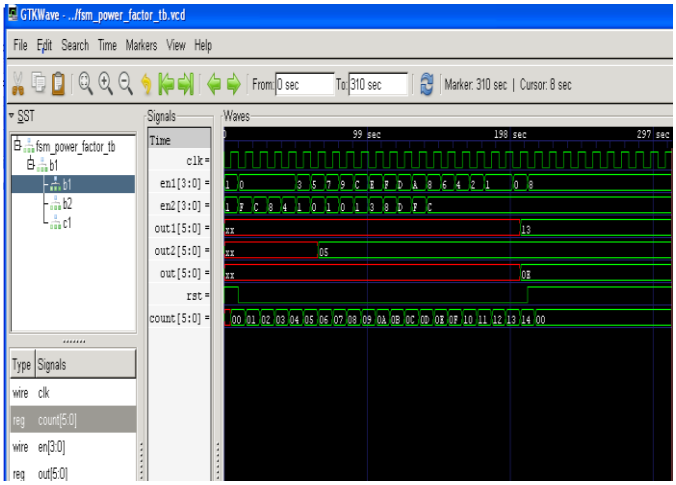

Fig.7: Simulation result of the system in I-verilog

The output of the power factor correction technique are given to the capacitor banks to improve the power factor. Fig.8 shows synthesis result for the PFC. The following reports have been generated:

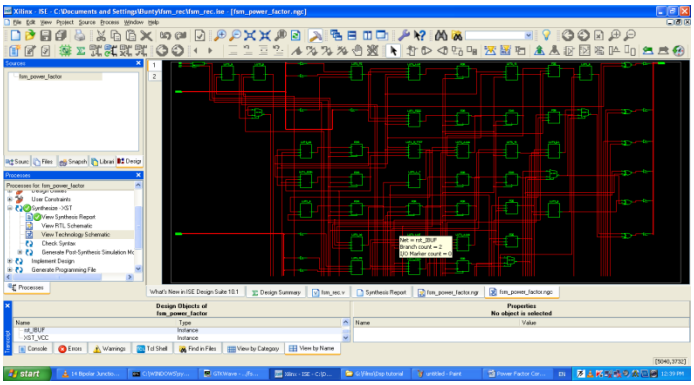

Fig.8: Synthesis view of the system

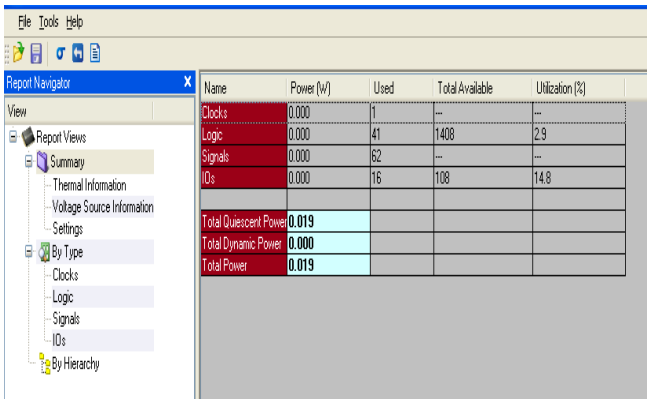

Fig.9: Power report of the system

Final Results
RTL Top Level Output File Name : fsm_power_factor.ngr
Top Level Output File Name : fsm_power_factor
Output Format : NGC
Optimization Goal : Speed
Keep Hierarchy : NO

Design Statistics
IOs : 16

Cell Usage:
BELS : 59
LUT2 : 13
LUT2_L : 2
LUT3 : 13
LUT4 : 11
LUT4_D : 2
MUXCY : 11
VCC : 1
XORCY : 6
FlipFlops/Latches : 28
FDE : 12
FDR : 16
Clock Buffers : 1
BUFGP : 1
IO Buffers : 15
IBUF : 9
OBUF : 6
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Device utilization summary:

Selected Device : 3s50antqg144-5

Number of Slices:	24	out of	704	3%
Number of Slice Flip Flops:	28	out of	1408	1%
Number of 4 input LUTs:	41	out of	1408	2%
Number of IOs:	16			
Number of bonded IOBs:	16	out of	108	14%
Number of GCLKs:	1	out of	24	4%

7. CONCLUSIONS

A hardware implemented FPGA-based power factor correction technique has been proposed for receiving substations in this paper. The device enables to keep the power factor near unity (within close bounds) by switching on or off elements of a 3-phase capacitor bank. It has the merits of accuracy and fast inference speed. In addition, it is easily integrated into existing systems, and is adaptive to network reconfiguration. The scheme extracts information from voltage and current signals to detect the power factor and improve the same. The logic is easily comprehensible, deterministic and is implemented using SPARTAN3AN FPGA kit. FPGAs provide an affordable, customised option for testing the performance of new protection techniques. The prototype has been developed to evaluate the performance of the proposed logic in real-time.

The logic for power factor correction circuit has realized using block diagram as well as using state diagram in this paper. Future work may include a VLSI implementation of the proposed architecture.

8. References

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